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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/114,203	07/13/98	MIYANISHI A	030682-066

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BAUMEISTER, B	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/114,203	Miyanishi et al.
Examiner	**Art Unit**
William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 19, 2001* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above, claim(s) *2-11* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1 and 12* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *17*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jassowski '389. As was explained in the previous Office Actions (paper #10 dated 8/4/2000 and paper #15 dated 3/5/2001) Jassowski teaches isolated active regions in which are provided a plurality FETs having gate electrodes with end caps. One such active region includes an ordinary region having a gate 2 (as numbered by the present applicant) with an end cap length x and a depressed region having a gate 1 with an end cap length $x + \alpha$.

a. Jassowski does not teach the added limitation (amendment B, paper #11) relating to the relative lengths of the end-cap margins: i.e. $0 < \alpha \leq x$. But it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Thus, patentability of the present claims depends on whether the relationship, $0 < \alpha \leq x$, produces a patentable difference over Jassowski, or in other words, whether this claimed relationship between x and α produces some additional unexpected result given Jassowski's teaching that the length of end cap 1 is longer than that of end cap 2.

b. Applicant has not set forth any explanations for the position that limiting the relationship between x and $x + \alpha$ to $0 < \alpha \leq x$ somehow better achieves the invention's primary goal of preventing shorting between the FET's source/drain regions, or achieves any other purpose or goal. Further, no portion of the specification sets forth any unexpected results obtained by setting the relationship to $0 < \alpha \leq x$. Rather, the specification indicates that this relationship is a mere design choice involving routine skill in the art. See for example, page 17, line 23 - page 18, line 9 of the specification, reciting:

> A gate end cap (margin part) of the gate electrode has a length x. This gate end cap is set as the margin part (gate portion extending beyond the active area) in order to prevent the length of the gate electrode from being reduced below the span of the active area. The length x is so set that a forward portion of the gate electrode is not located on the active area even if this forward end portions is rounded due to corrosion by etching or the like to partially reduce the gate length. The length x of the gate end cap of the gate electrode 20 is set as that from an edge portion of the active area on layout design.
>
> On the other hand, a gate end cap of the gate electrode 30 has a length $x + \alpha$. The additional length α is set to be not more than the length x of the gate end cap of the gate electrode arranged on the ordinary region ($0 < \alpha \leq x$), *for example (emphasis added).*

This disclosure indicates that the goal sought to be achieved is to prevent the shorting of the source/drain in the FET of the depressed region by making the end cap length of the depressed region FET's sufficiently long. The use of the term "for example" indicates that this specific relationship in length, $0 < \alpha \leq x$, is merely one possible way of preventing the shorting, but that it is not at all necessary to satisfy this relationship to achieve this goal. Further, other portions of the specification support the Examiner's position that the relationship $0 < \alpha \leq x$ is merely a design

choice, not leading to any unexpected results. See, for example, various alternative embodiments which also achieve the same goal, but wherein w (or α) $\geq$ x (FIG 3) and wherein α = x (FIGs 6 and 15).

c. Moreover, the fact that Jassowski does not discuss the prevention of current leakage, much less adjusting these relational lengths as discussed above for the specific purpose of preventing current leakage, is immaterial. This would also have been equally true even if Applicant had provided some rationale for why limiting the respective lengths to the relationship 0 $< \alpha \leq$ x provides some unexpected result. Specifically, such factors are immaterial to the issue of whether the claims are rendered obvious by Jassowski if some independent motivation existed at the time of the invention for modifying the structures taught by Jassowski such that they satisfy each claim's limitation regarding the margin's relative lengths. This is because it has been held that the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Jassowski teaches that active areas having portions with different channel widths (ordinary and depressed regions) may be provided with gates in the respective regions having end caps that terminate at the same imaginary line (hereinafter referred to as "co-extensive end cap terminations") (see gates "1" and "2" as labeled by Applicant). Thus, the pending claims would be rendered obvious by Jassowski if motivation existed at the time of the invention to modify the

respective channel widths of the ordinary and/or depressed regions such that the resulting structure satisfies the relationship as claimed: i.e., modifying the active area such that α, the difference in channel width between the ordinary region and the depressed region, is less than x. This could be accomplished by either increasing the channel width of the depressed region, by decreasing the width of the ordinary region, or a combination of the two. It was known to those of ordinary skill in the art at the time of the invention that increasing the channel width of a FET increases conductivity, while decreasing the channel width increases resistance and saves space. Thus, in light of the Jassowski teachings, it would have been obvious to one of ordinary skill in the art at the time of the invention that the gate widths of such an active area's ordinary and depressed regions can be adjusted to any of various lengths and relative relationships while maintaining co-extensive end cap terminations, including those wherein $0 < \alpha \leq x$, for the purpose of adjusting the respective FETs conductivities and space requirements, the specific lengths ultimately chosen depending only upon conventional design considerations such as the specific transistor sizes and resultant circuit desired and the available chip space. In other words, it would have been obvious to one of ordinary skill in the art at the time of the invention that the differential channel width "α" could be set to any desired length including $\alpha \leq x$ depending only upon conventional design considerations.

Response to Arguments

3. Applicant's arguments filed 6/19/01 have been fully considered but they are not persuasive for the reasons set forth previously, above and as follows:

a. Applicant asserts that claims 1 and 12 were rejected under 35 U.S.C. § 103 as being anticipated by Jassowski et al." (REMARKS, paper #16, page 3, next to last paragraph). This is clearly a clerical error, but to clarify the record, the Examiner notes that the claims were rejected as being obvious over--not anticipated by--Jassowski.

b. Applicant argues that Jassowski is directed towards space-saving measures that are unrelated to the problem of current leakage at gate margins formed in a depressed region, and that nothing in Jassowski shows, teaches or suggests how to prevent this current leakage by forming a larger gate cap length for the gate in the depressed region than that in the ordinary region by a length of $x + a$ where $0 < a \leq x$, as set forth in claims 1 and 12 (REMARKS at page 4). The Examiner agrees that the problems to be solved by Jassowski are unrelated to the problem to be solved by applicant. However, this is immaterial because the claims are nonetheless rendered obvious over Jassowski for at least the reasons set forth above. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

c. Regarding the argument that end cap "3" is longer than that of end cap "2" and therefore teaches away from the invention, the examiner disagrees. Initially, it is not clear to the Examiner that end cap 3 is, in fact, longer than end cap "2." Rather, they seem be of approximately equal length. Regardless, and under either interpretation, the fact that this one end

cap may be the same length as or longer than this other one does not teach away from the present invention. Instead, it merely supports the Examiner's position that the specific choice of a particular end cap length is not tied to the particular width of the associated channel, but rather, the lengths can be chosen independently based on other conventional design considerations such as space, layout, masking or etching requirements.

4. As claims 1 and 12 remain rejected, the issue of rejoinder of any other claim(s) is moot.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. William Baumeister

July 9, 2001

Jerome Jackson, Jr.
Primary Examiner